ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	STRUCTURE AND METHOD OF MAKING A BIPOLAR TRANSISTOR HAVING REDUCED COLLECTOR-BASED CAPACITANCE

Application Number : 10/708,860

Confirmation Number:

First Named Applicant: Hiroyuki Akatsu

Attorney Docket Number: FIS920030415US1

Art Unit: 2818

Examiner: Dao Nguyen

Search string: (5494836 or 5506427 or 5962880 or 6346453 or 5128271 or 20030057458 or 20030109109).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
dlw	1	5494836	1996-02-27	Imai			
	2	5506427	1996-04-09	Imai			
	3	5962880	1999-10-05	Oda, et al.			
	4	6346453	2002-02-12	Kovacic, et al.			
dlw	5	5128271	1992-07-07	Bronner, et al.			

US Published Applications

Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
dlw	1	20030057458	2003-03-27	Freeman, et al.			
dlw	2	20030109109	2003-06-12	Freeman, et al.			

Signature

Examiner Name	Date
Dao	11/11/05